APx PDM Option: Technical Details

Table of Contents

Introduction

The APx PDM option is a module for the APx 525, 526, 555, 582, 585, and 586 audio analyzers. It can generate a high quality stereo PDM signal, and analyze a stereo PDM signal. It features a power supply output for powering the connected device under test (DUT). This supply can be modulated automatically to measure power supply rejection (PSR).

This document describes in detail the features and operation of the APx PDM option. It is intended primarily for designers of PDM devices. For an introduction to the basics of PDM, please see the Audio Precision white paper, "Understanding PDM Audio" (http://www.ap.com/display/file/612). Complete specifications are available at http://www.ap.com/display/file/656. Additional information is available on the PDM Option product page (http://www.ap.com/products/apx/pdm).

General Architecture

The PDM module plugs into a full-size APx instrument. Like all APx modules, it connects to the system through a backplane that sends audio test signals in PCM form to the module, receives audio signals from the module, and provides clock and control lines. APx is at heart a PCM system. The PDM module converts PCM from the APx waveform generator to PDM on the transmitter side, and converts PDM to PCM on the receiver side for analysis. The signals are kept in the digital domain at all times.

Because PDM devices accept a range of power supply and logic levels, the module is equipped with a dual programmable DAC-based power supply. One supply powers the internal interface logic, while the other drives the 'VDD' BNC jack on the front panel for powering devices. The signal on the VDD port can be modulated to measure the PSR of the device. This modulation does not affect the internal logic levels or thresholds.

The transmitter and receiver are completely independent (apart from the logic level, which is the same for both). The system can operate with both transmitter and receiver active, with independent selection of the clock direction and at independent clock rates.

On the output side, the conversion from PCM to PDM is performed by an interpolator and a PDM modulator. On the input side, a decimator converts PDM to PCM. The interpolation and decimation ratios can be chosen independently. There is also a decimator bypass mode in which the raw PDM signal is passed to the application for analysis. This allows developers of PDM devices to see the full spectrum produced by the modulator. This is invaluable for checking performance above the audio band.

The entire PDM engine is implemented in an FPGA. The FPGA code is downloaded at boot time. Therefore it is possible to add more features in future software releases.

Transmitter Side (Generator)

Interpolation Filter

The transmitter consists of a stereo interpolating digital filter which feeds a high performance stereo PDM modulator. The interpolation filter main specifications are as follows[1]:

- Interpolation ratios (INTR): 16, 16.67, 21.33, 24, 25, 32, 33.33, 37.5, 42.67, 48, 50, 62.5, 64, 66.67, 75, 85.33, 96, 100, 125, 128, 150, 192, 200, 250, 256, 300, 384, 400, 500, 512, 600, 768, 800
- Passband: DC to 0.45 f_s, where f_s is the decimated rate
- Passband gain, power of two INTR values: ±0.0001 dB
- Passband gain, all other INTR values: +0.0001 dB, -0.0063 dB
- Stopband attenuation, power of two INTR values: 115 dB minimum
- Stopband attenuation, all other INTR values: 100 dB minimum

The following decimation ratios are true rationals, with values as shown:

Displayed DECR	Actual DECR
33.33	100/3
42.67	128/3
66.67	200/3
85.33	256/3

The interpolation filter is fed with 24-bit dithered PCM audio. The wordlength and dither are internally set and cannot be changed by the user[2]. All of the test signals generated by APx can be used, including sine waves, multitones, chirps, and more. Arbitrary waveforms can also be played over the PDM interface. It is not possible to play bit-exact or digitally encoded waveforms, because the interpolation and wordlength reduction that are at the heart of PDM do not retain bit exactness.

PDM Modulator

The PDM modulator main specifications are as follows:

- Modulator order: 4 or 5
- Designed oversampling ratios: 64x, 128x, 256x, 512x
- Passband gain: 0 dB
- Ones density at 0 dBFS: 100 %
- Fourth-order modulator, 64x oversampling ratio, 48 kHz baseband rate:
    - Overload point: -7.8 dBFS
    - THD+N ratio @ 1 kHz, -7.8 dBFS, 20 Hz – 20 kHz, unweighted: -105 dB
    - Dynamic range @ 1 kHz: 115 dB (per AES17)

[1] See the Technical Specifications document for full details.
[2] There is no use case for feeding the PDM system with anything less than the highest quality audio.

- Fifth-order modulator, 256x oversampling ratio, 48 kHz baseband rate:
    - Overload point: -9.8 dBFS
    - THD+N ratio @ 1 kHz, -9.8 dBFS, 20 Hz – 20 kHz, unweighted: -128 dB
    - Dynamic range @ 1 kHz: 137 dB (per AES17)

For the fourth order modulators, the noise floor in the passband is largely white, except for the presence of two dips in the upper band. See Figure 1, below. The dips are caused by zeros in the modulator's noise transfer function. These zeros are deliberately placed to keep the noise power as low as possible across the passband. The signal transfer function (that is, the frequency response of the modulator) is always unity and is unaffected by these zeros.

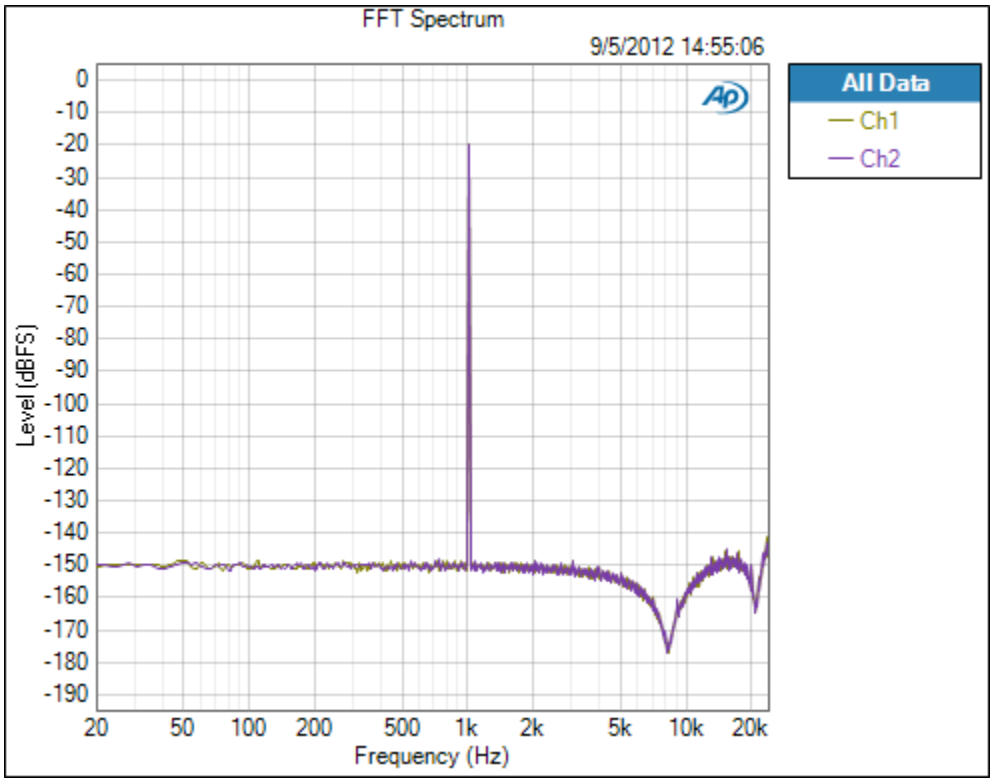

Figure 1: Passband noise floor of 4th order modulator (64x interpolation ratio, 48 kHz sampling rate). Signal is 1 kHz, -20 dBFS.

The dips are difficult to see for modulators with an oversampling ratio higher than 64x, because the noise floor is so low that its features are masked by the dither floor and the roundoff error in the interpolation and decimation filters.

The fifth-order modulators have an additional zero at DC in the noise transfer function. This causes the noise spectrum to have a 6 dB/octave highpass characteristic, in addition to the dips in the upper band. At low frequencies, this rolloff is masked by the dither floor and the roundoff error in the interpolation and decimation filters. See Figure 2, below.

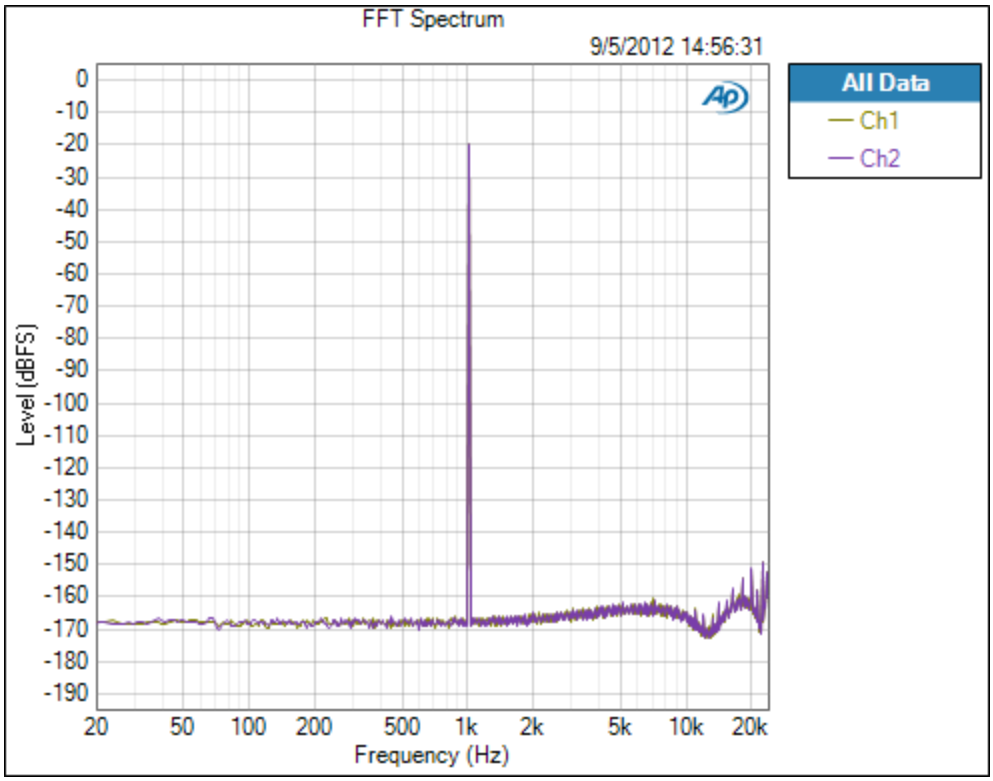

Figure 2: Passband noise floor of 5th order modulator (64x interpolation ratio, 48 kHz sampling rate). Signal is 1 kHz, -20 dBFS.

The modulators generate a small amount of mostly third harmonic distortion. This is an unavoidable consequence of reducing the wordlength to one bit while keeping the noise floor very low. See Figure 3. If the third harmonic product falls into one of the noise floor dips, its level will be reduced by the same factor by which the noise is reduced in the dip. See Figure 4. The 5th order modulators generate negligible distortion. See Figure 5.

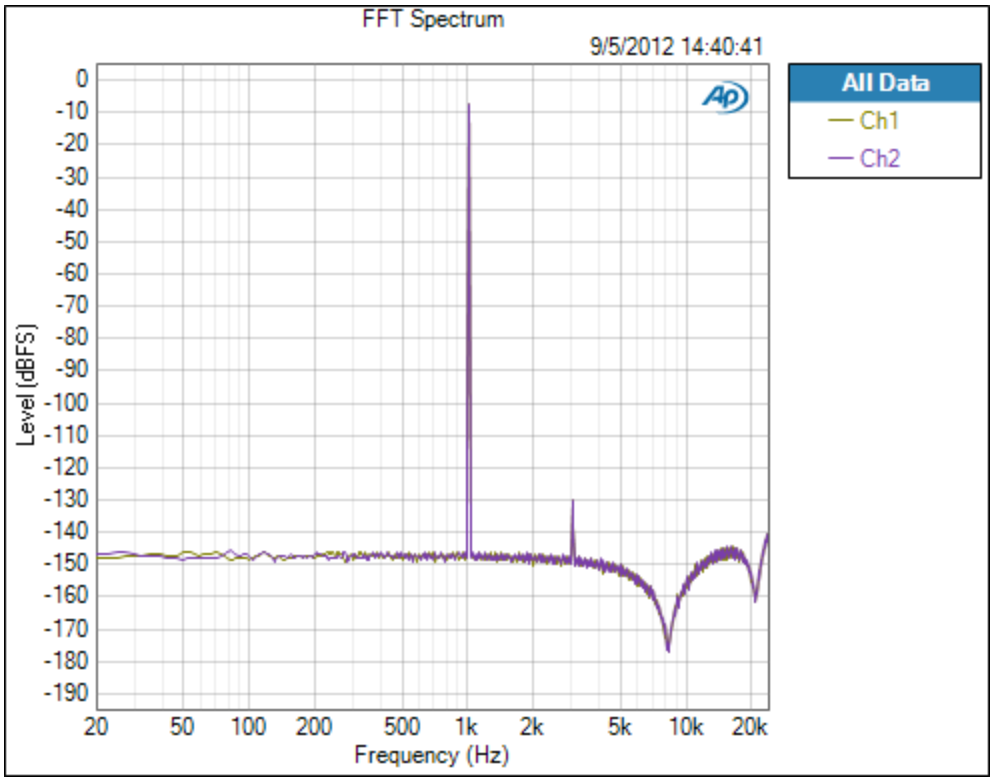

Figure 3: 1 kHz signal at -7.8 dBFS, showing third harmonic at -122 dB relative to the fundamental (4th order modulator, 64x interpolation ratio).

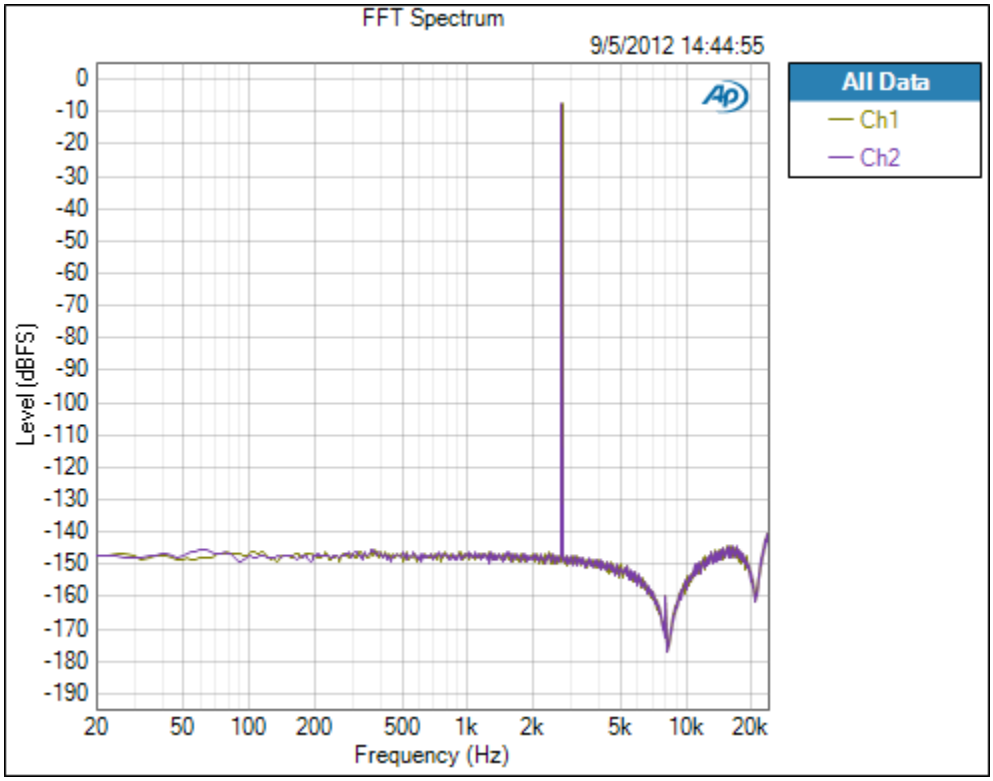

Figure 4: 2.68 kHz signal at -7.8 dBFS, showing suppression of third harmonic by zero in the noise transfer function.

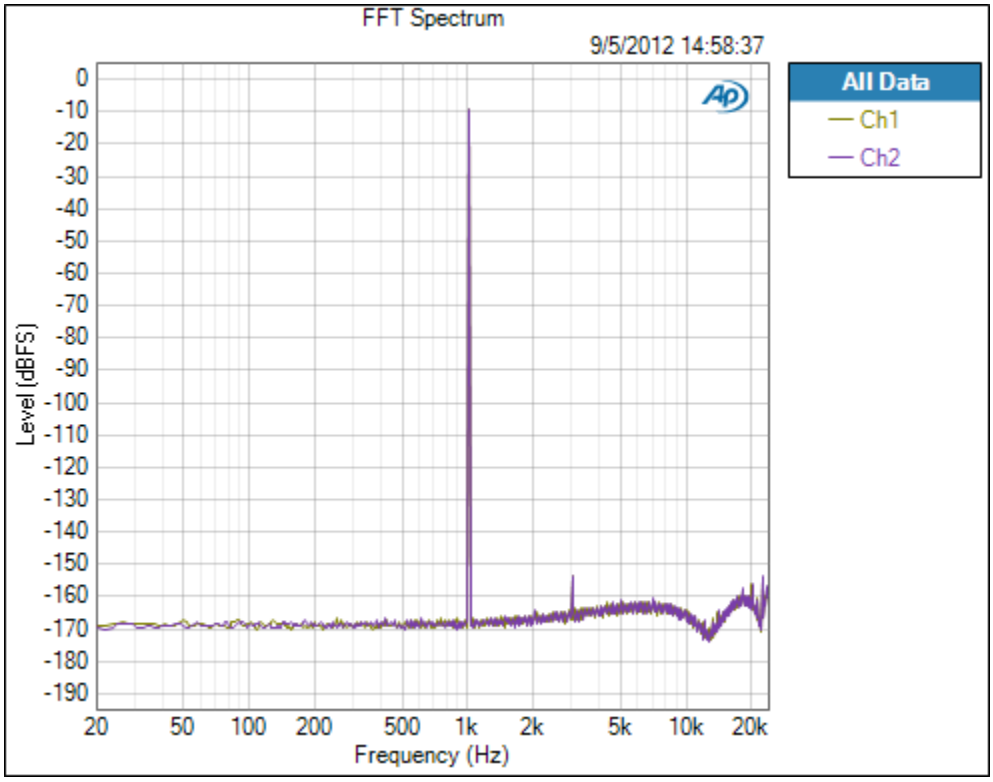

Figure 5: 1 kHz signal at -9.8 dBFS, showing very low third harmonic distortion (5th order modulator, 64x interpolation ratio).

Overload Point

All high-order one-bit modulators have a maximum input signal level above which the modulator becomes overloaded[3]. The APx modulators are designed to operate at moderate overload without performance degradation. At signal levels approaching digital full scale, noise and distortion performance become increasingly degraded, with THD+N reaching around 2 % at 0 dBFS. However, the modulators remain stable, and the output signal level increases linearly with the input signal, reaching 100 % ones density at the peaks of a 0 dBFS signal.

The best THD+N performance is achieved for signal levels close to the overload point[4]. Modulator overload is detected at the quantizer and is indicated in the UI status bar (see Figure 6), to aid in setting the generator level. Occasional mild overloads will not materially affect measurements.

[3] Overload occurs when the signal level at the quantizer input is outside the range of the two quantization levels.
[4] See the specifications document for the overload point of each modulator.

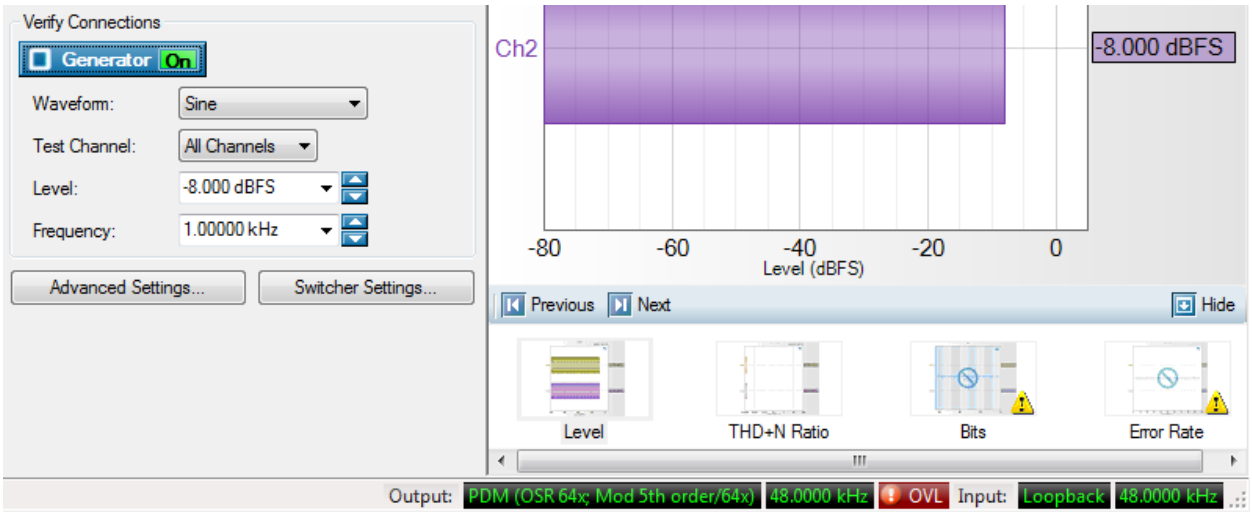

Figure 6: Modulator overload is indicated in the status bar with a red "OVL" flag.

Bit Clock and Decimated Rate

Most devices designed to receive PDM signals supply the bit clock to the transmitter. That is, the transmitter is typically configured as a slave. The APx option allows the transmitter to be a slave or a master. The bit clock direction is set in Signal Path Setup. See Figure 7. The 'Bit Clk Dir' control sets the bit clock direction.

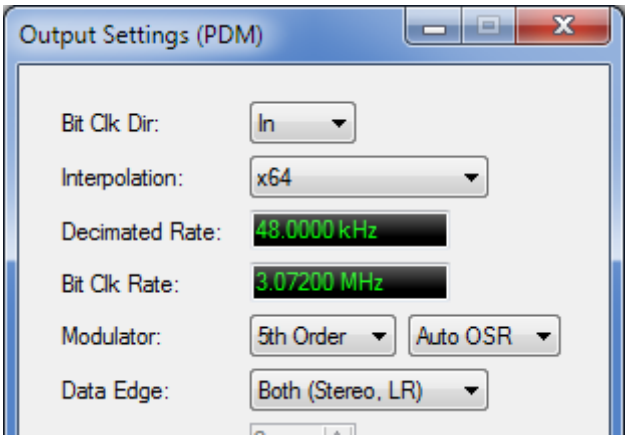

Figure 7: PDM output settings in Signal Path Setup (configured as a slave).

When the APx is a slave, the bit clock rate is set by the receiver. The bit clock rate is shown in the settings dialog. When APx is a master, the user sets the decimated rate. The derived bit clock rate is shown in the dialog.

Interpolation Ratio and Modulator Order

Fourth and fifth order modulators for oversampling ratios of 64x, 128x, 256x, and 512x are included. The choice of modulator is automatic according to the choice of interpolation ratio, or can be overridden by the user.

In the automatic mode (selected by choosing 'Auto OSR' for the modulator, as shown in Figure 7), the 64x modulator is used for interpolation ratios of 64x and below. The 128x modulator is used for ratios between 66.67 and 128. The 256x modulator is used for ratios between 150 and 256. The 512x modulator is used for all higher ratios. In the manual mode, the user chooses which modulator to use.

The decimated rate is limited to the range 4 kHz to 216 kHz. In addition, the bit clock is limited to 24.576 MHz maximum. At oversampling ratios of 128x and above, therefore, the maximum decimated rate is limited by the bit clock.

Interfacing

The embedded audio on the data line can be mono or stereo. The "Data Edge" choice in the settings panel allows the user to select whether the output is mono or stereo.

In mono mode, the user selects whether the rising or falling edges of the bit clock are modulated. The chosen edges are modulated by generator Channel 1. The opposite edge is unmodulated. Please note that the unmodulated edge is not tri-stated. It is therefore not possible to wire-OR the data line with another PDM source.

In stereo mode, both edges are modulated. In "Stereo, LR" mode, Channel 1 of the generator modulates the rising edge, while Channel 2 modulates the following falling edge. In "Stereo, RL" mode, Channel 1 of the generator modulates the falling edge, while Channel 2 modulates the following rising edge.

Logic Level

The Logic Level control determines the level at which the internal interface logic operates. This in turn sets the following:

- The data output high level. Low level is always 0 V.
- In clock master mode, the bit clock high level. Low level is always 0 V.
- In clock slave mode, the low/high threshold for the bit clock input. This threshold is always half way between 0 V and the logic level. There is approximately 50 mV of hysteresis.

Vdd Level and DC Power On/Off

The external V_{DD} connector can be used to power the device under test. This simplifies hookup, and allows the power supply rejection (PSR) of the device to be measured. The V_{DD} connector is described in detail in the receiver section.

Receiver Side (Analyzer)

Decimation Filter

The receiver consists of a stereo decimating digital filter. The decimation filter main specifications are as follows:

- Decimation ratios (DECR): 1, 3.125, 4, 6.25, 8, 8.33, 10.67, 12.5, 16, 16.67, 18.75, 21.33, 24, 25, 32, 33.33, 37.5, 42.67, 48, 50, 62.5, 64, 66.67, 75, 85.33, 96, 100, 125, 128, 150, 192, 200, 250, 256, 300, 384, 400, 500, 512, 600, 768, 800

- Passband: DC to 0.45 f_s, where f_s is the decimated rate
- Passband gain, power of two DECR values: ±0.0001 dB
- Passband gain, all other DECR values: ±0.001 dB
- Stopband attenuation: Better than 120 dB

The following decimation ratios are true rationals, with values as shown:

Displayed DECR	Actual DECR	Displayed DECR	Actual DECR
8.33	25/3	33.33	100/3
10.67	32/3	42.67	128/3
16.67	50/3	66.67	200/3
21.33	64/3	85.33	256/3

The output of the decimation filter is PCM. It is analyzed by the APx system just like any other signal source. This allows advanced measurements such as multitones and chirps to be performed.

Bitstream (1x) Mode

When designing a PDM modulator, it is important to examine not just the audio (baseband) performance, but also the characteristics of the modulator in the stopband, where most of the noise shaping occurs. The APx PDM option allows the entire PDM signal to be examined, using the '1x' decimation ratio[5]. Figure 8 shows an example.

[5] In earlier versions of the software, bitstream (1x) mode was only available in the Signal Analyzer measurement. Current software retains this feature, and adds 1x as a decimation ratio in its own right. This allows any measurement to be made on the bitstream.

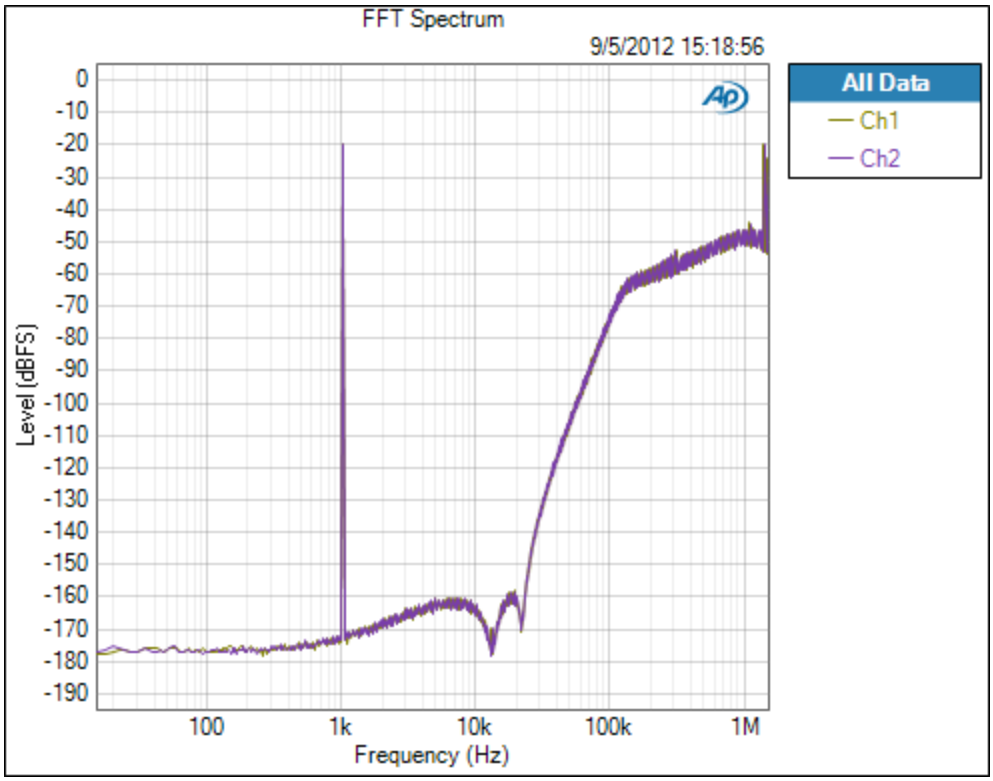

Figure 8: "PDM Bitstream" mode power spectrum (5th order modulator, 64x interpolation ratio, 48 kHz decimated rate).

The vary large FFT sizes available in Signal Analyzer (up to 1.2 million points) allow even the wideband PDM bitstream signal to be analyzed at very high resolution. Averaging can also be used. The signal can be examined in the time and frequency domains, and spectral density views are also shown.

Bit Clock and Decimated Rate

Most devices designed to transmit PDM signals accept the bit clock from the receiver. That is, the receiver is typically configured as a master. The APx option allows the receiver to be a master or a slave. The bit clock direction and the decimated rate are set in Signal Path Setup. See Figure 9.

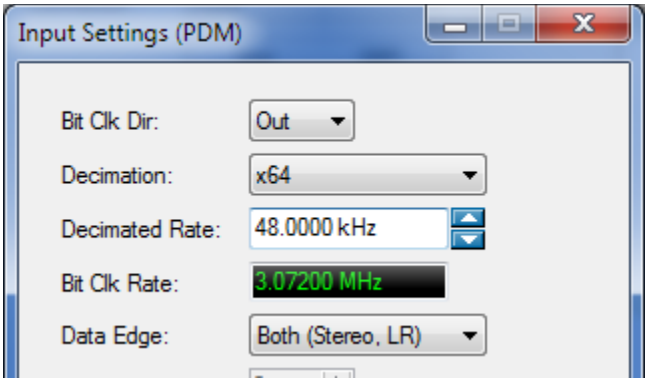

Figure 9: PDM input settings in Signal Path Setup (configured as a master).

Decimation Ratio

The “Decimation” control determines the decimation ratio. The decimated rate is the bit clock rate divided by the decimation ratio.

Interfacing

The PDM audio received by APx can be mono or stereo. The “Data Edge” choice in the settings panel allows the user to select whether to demodulate the data on the rising edge of the bit clock (mono), the falling edge (also mono), or both edges (stereo).

In mono mode, the demodulated data always becomes analysis Channel 1, regardless of the edge chosen.

In stereo mode, both edges are demodulated. In “Stereo, LR” mode, the rising edge data becomes analysis Channel 1, while the following falling edge data becomes analysis Channel 2. In “Stereo, RL” mode, the falling edge data becomes analysis Channel 1, while the following rising edge data becomes analysis Channel 2.

Mono PDM devices support stereo by asserting the data line on one clock edge, and tri-stating it on the other. A pin selects the active edge. Two devices with opposite active edges can then simply have their data lines wire-ORed. If a single stereo-capable device is connected to the APx, then depending on the impedances and timing, APx may be able to read the PDM data on both clock edges. Selecting ‘Rising’ or ‘Falling’ for the Data Edge will then make no difference. (Selecting either of the stereo modes will result in two identical channels of audio.) This is not a malfunction, either of the device under test or the APx.

Logic Level

The Logic Level control determines the level at which the internal interface logic operates. This in turn sets the following:

- The low/high threshold for the data input. This threshold is always half way between 0 V and the specified logic level. There is approximately 50 mV of hysteresis.
- In clock master mode, the bit clock high level. Low level is always 0 V.
- In clock slave mode, the low/high threshold for the bit clock input. This threshold is always half way between 0 V and the specified logic level. There is approximately 50 mV of hysteresis.

Vdd Level and DC Power On/Off

The external V_{DD} connector provides power to the device under test. The power requirements of most devices (such as PDM microphones) are small and well within the capability of the APx power output. The V_{DD} level is set independently of the interface logic level.

Power Supply Rejection Measurements

The APx PDM option is able to modulate the V_{DD} level. This allows the power supply rejection (PSR) of a device to be measured directly. (Only the level on the V_{DD} connector is modulated. The internal logic levels do not vary.) The PSR measurements co-opt the APx generator to modulate the V_{DD} level. The

audio on the currently selected audio interface (if any) is muted, although the interface itself remains active.

The application software has two measurements dedicated to measuring PSR. Both are available regardless of the choice of input connector. This allows PSR measurements to be made on devices with analog or I^2S interfaces, as well as those with PDM interfaces, as long as the device can be powered from the V_{DD} port.

The **PSR** measurement measures the PSR of the device at a single frequency. V_{DD} can be modulated with several classes of waveforms; the analysis follows the waveform choice. They are:

- **Square wave**. V_{DD} is modulated with a 217 Hz square wave whose peak level is set by the user (default 100 mVpp)[6]. The analysis uses window-width bandpass filters placed at the fundamental and its odd harmonics, up to the 101st. The PSR is the RMS sum of the levels inside the bandpass filters. The sum can be frequency weighted, if desired.
- **Pulse wave**. V_{DD} is modulated with a 217 Hz pulse wave whose peak level is set by the user (default 100 mVpp) and duty cycle (from 1/8 to 7/8, in steps of 1/8)[7]. The analysis uses window-width bandpass filters placed at the fundamental and its harmonics, up to the 101st. The PSR is the RMS sum of the levels inside the bandpass filters, optionally frequency weighted.
- **Sine wave**. V_{DD} is modulated with a sine wave at a user-set frequency and level. The analysis uses a window-width bandpass filter placed at the fundamental. The PSR is the RMS level inside the bandpass filter, optionally frequency weighted.
- **Noise**. V_{DD} is modulated with a pseudo-random noise waveform having a triangular probability density function and a peak level set by the user. The PSR is the RMS level of the input signal, optionally frequency weighted.

The use of window-width filters provides a low-noise estimate of the PSR, since the power outside the filters is rejected. This enables PSR measurements to be made on microphones which are not in an acoustically quiet environment. Regardless of the waveform choice, a PSR+N result is also available. This is simply the weighted level of the input signal[8].

The PSR and PSR+N results are expressed in dBFS (for digital inputs) or dBV (for analog inputs). For analog inputs, PSRR and PSRR+N results are also available. These are the ratio between the RMS level of the V_{DD} modulation to the PSR and PSR+N results, respectively. The RMS level of the V_{DD} modulation is computed from the user-set generator level and the waveform type.

[6] This is a typical configuration for measuring PSR in microphones designed for mobile applications. Square wave modulation of the power supply simulates the digitally noisy environment of a GSM mobile phone. The actual frequency of the square wave is the GSM frame rate of 26 / 0.12 Hz (approximately 216.667 Hz).
[7] The pulse wave simulates GSM noise with a variable number of time slots used, from 1 to 8. Square wave mode covers the 4-slot case.
[8] For the noise waveform, PSR and PSR+N are identical.

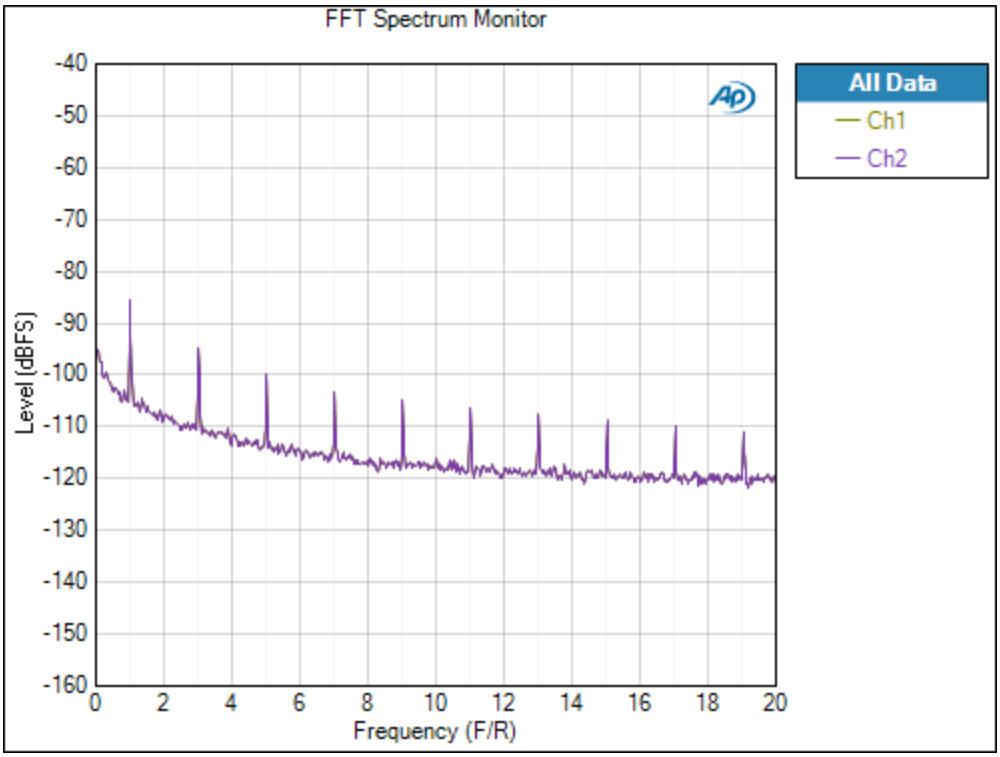

Figure 10: Spectrum of PDM MEMS microphone output when power supply is modulated with 100 mVpp square wave at 217 Hz. The x-axis is the harmonic number. Odd harmonics are summed to compute the PSR in square wave mode.

The **PSR Frequency Sweep** measurement measures the PSR of the device across the audio frequency band. This measurement is performed with sine waves. The user sets the start and stop frequencies, the number of points and their spacing, and the level of the sine wave. The analysis uses a window-width bandpass filter. The result can be frequency weighted if desired. A PSR+N result is also available. For analog inputs, PSRR and PSRR+N are also shown.

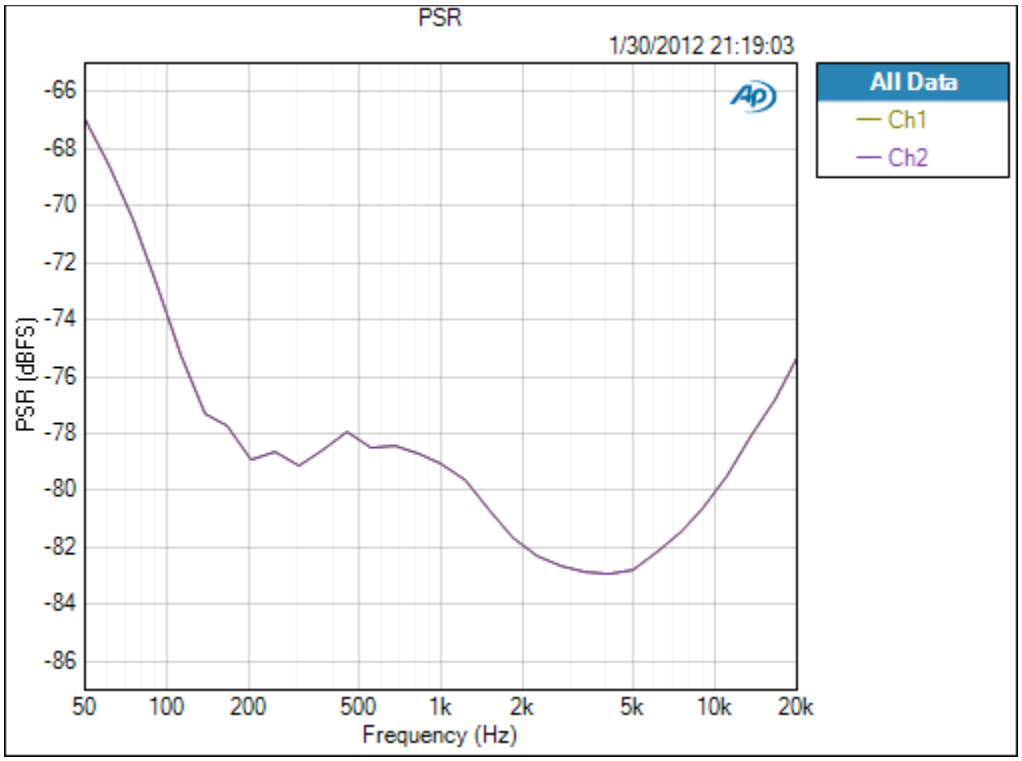

Figure 11: PSR measurement vs. generator frequency. The waveform is a sine wave at 100 mVpp.

Further Reading

The following additional documentation is available from the Audio Precision web site:

- Understanding PDM Audio (white paper) (http://www.ap.com/display/file/612)
- APx PDM Option Data sheet (http://www.ap.com/display/file/614)
- APx PDM Option Specifications (http://www.ap.com/display/file/656)
- Website: http://www.ap.com/produtcs/apx/pdm