Measuring Low-power ADCs with the APx555 ADC Test Option*

by Steve Peterson

This technote explains how to test a low power audio IC device with ADC Test option-equipped B Series APx555 audio analyzer (or Legacy APx555 with enhanced analog generator (EAG) upgrade).

ADC Test is a new optional feature of the APx555 analog balanced output that generates audio signals mixed with a calibrated common mode DC offset voltage. ADC Test is used to test a device that operates on a single supply voltage when the device inputs require a DC bias voltage set to ½ V_{DD}, such as audio codecs and analog-to-digital converter chips in mobile products.

Low power audio IC device analog audio inputs are configured by control register settings for differential and single-ended operation. These configurations support high-level signals for line input or low-level signals from MEMS microphones.

Figure 1 shows the different analog input configurations possible with a popular audio hub IC. V_{DD} is typically +1.8 V. The device's inputs can be configured for connections to microphones with differential or single-ended operation with high gain or can be configured as single-ended line level inputs with low gain.

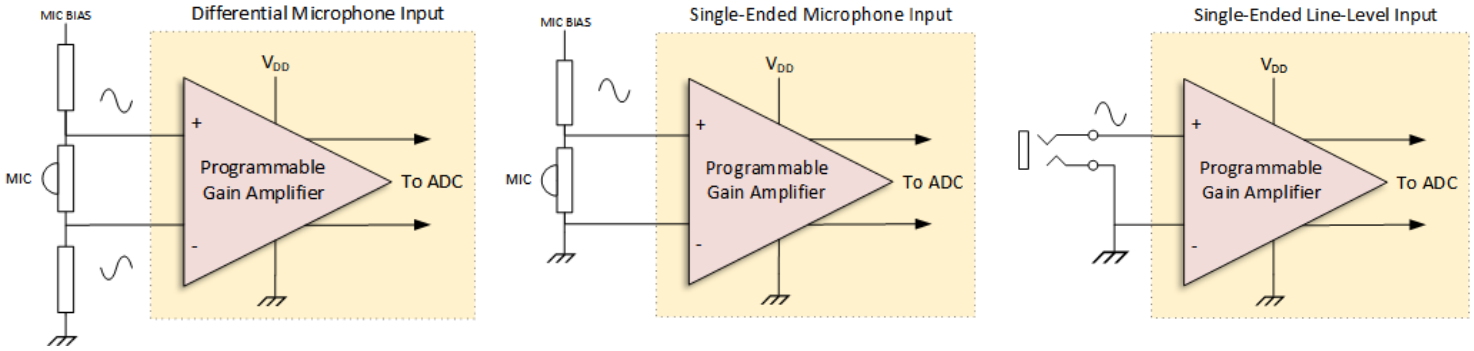

Figure 1. Direct coupled differential and single-ended inputs with single-supply V_{DD}. Optimal operation requires a DC bias of ½ V_{DD} on each active input pin.

Analog-to-Digital (ADC) Converter Measurements with VBias

An APx555 with the ADC Test option provides straightforward measurements on complex codecs, such as a Cirrus Logic CS47L90 audio hub IC. This IC provides configurable analog and PDM inputs for applications with microphones and line inputs; up to 7 analog, or 10 digital, microphone inputs and combinations of both. The analog inputs may be configured for both differential and single-ended inputs depending on the type of microphone element required.

Certain analog inputs can be re-tasked as two-channel digital microphone inputs (PDM). The APx555 is capable of generating analog and PDM signals simultaneously to test these mixed-mode inputs.

Let's test two of the DC-coupled analog input channels on the IC, one input configured as a differential low-level microphone input with high gain and the other configured as a single-ended line input with unity gain, shown in Figure 2.

*ADC Test Mode option requires either B Series APx555 or Legacy APx555 with EAG upgrade

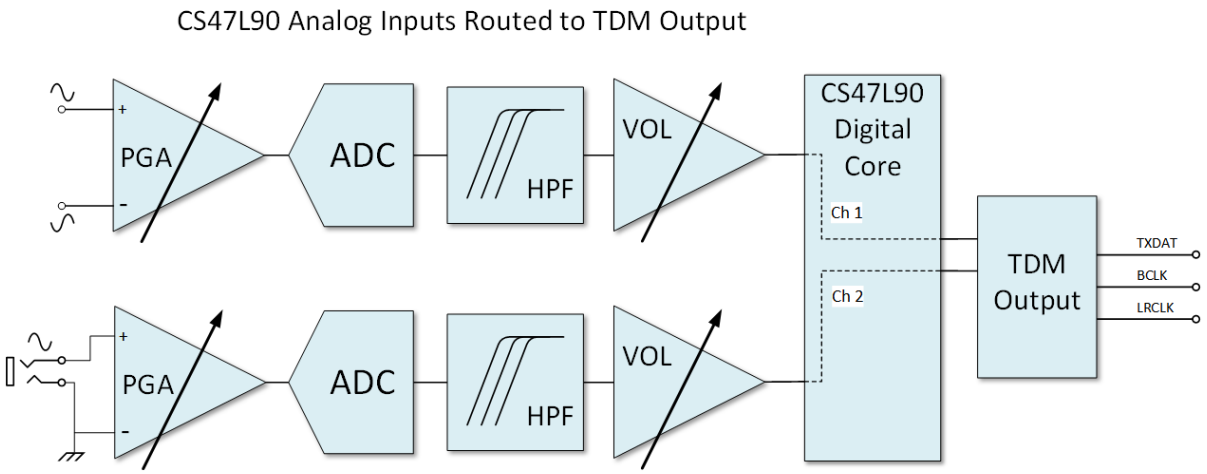

Figure 2. CS47L90 input 1 configured with both differential and single-ended analog inputs. The signals are routed through the digital core to a TDM output.

Figure 3 shows the CS47L90 evaluation board WISCE software setup necessary to achieve the configuration shown in Figure 2. The gain for the IN1BL differential input is set to +26 dB to produce full scale 0.0 dBFS output with 50 mVrms differential audio input. The gain for the IN1BR single-ended input is set to 0.0 dB to produce a 0.0 dBFS full scale output with a 500 mVrms single-ended audio input.

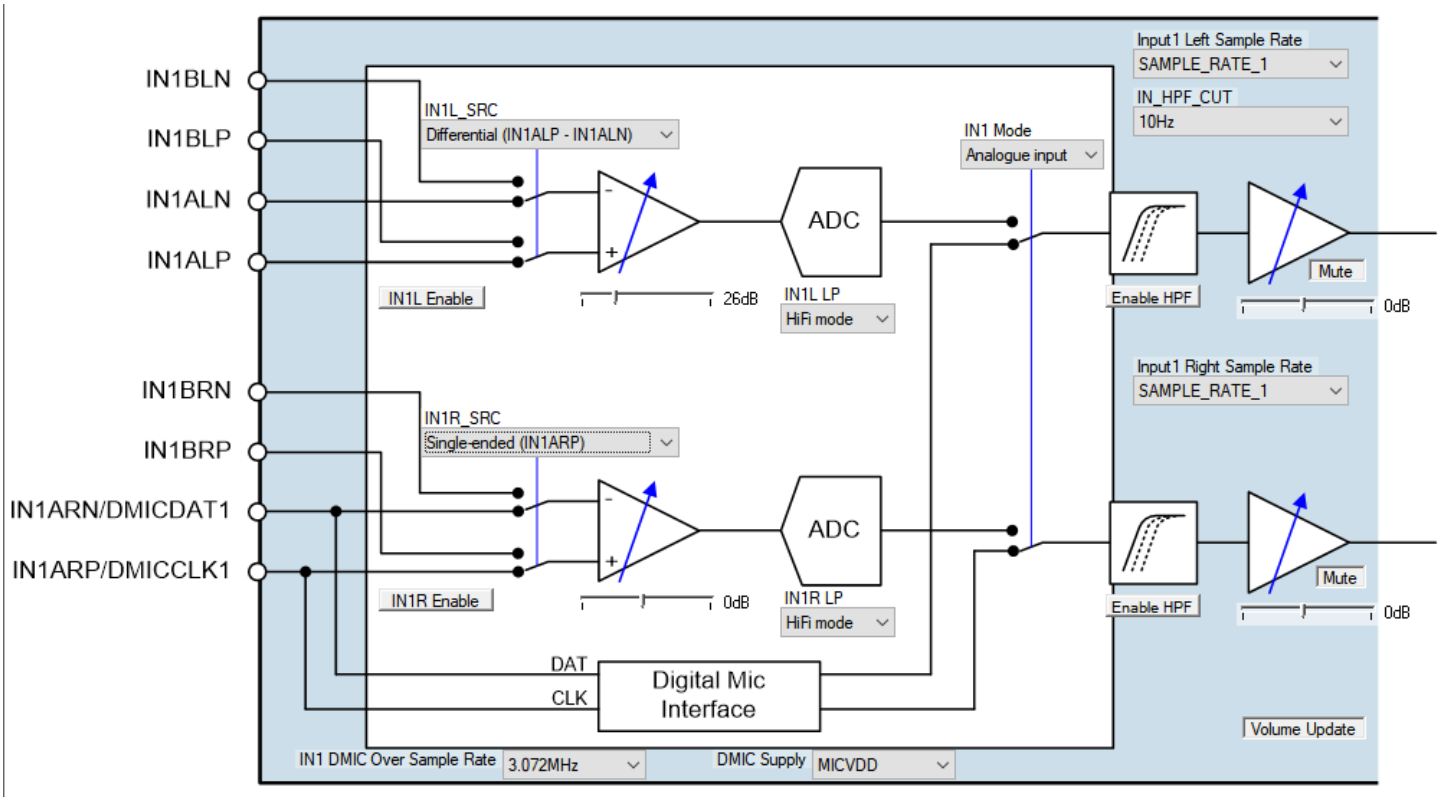

Figure 3. Cirrus Logic CS47L90 WISCE software evaluation board setup for two analog inputs. IN1AL set for +26 dB high gain differential microphone input with 50 mVrms full scale. IN1BR set for unity gain single-ended input with 500 mVrms full scale.

Figure 4 diagrams the signal connections between the APx555 and the CS47L90 analog inputs and TDM output.

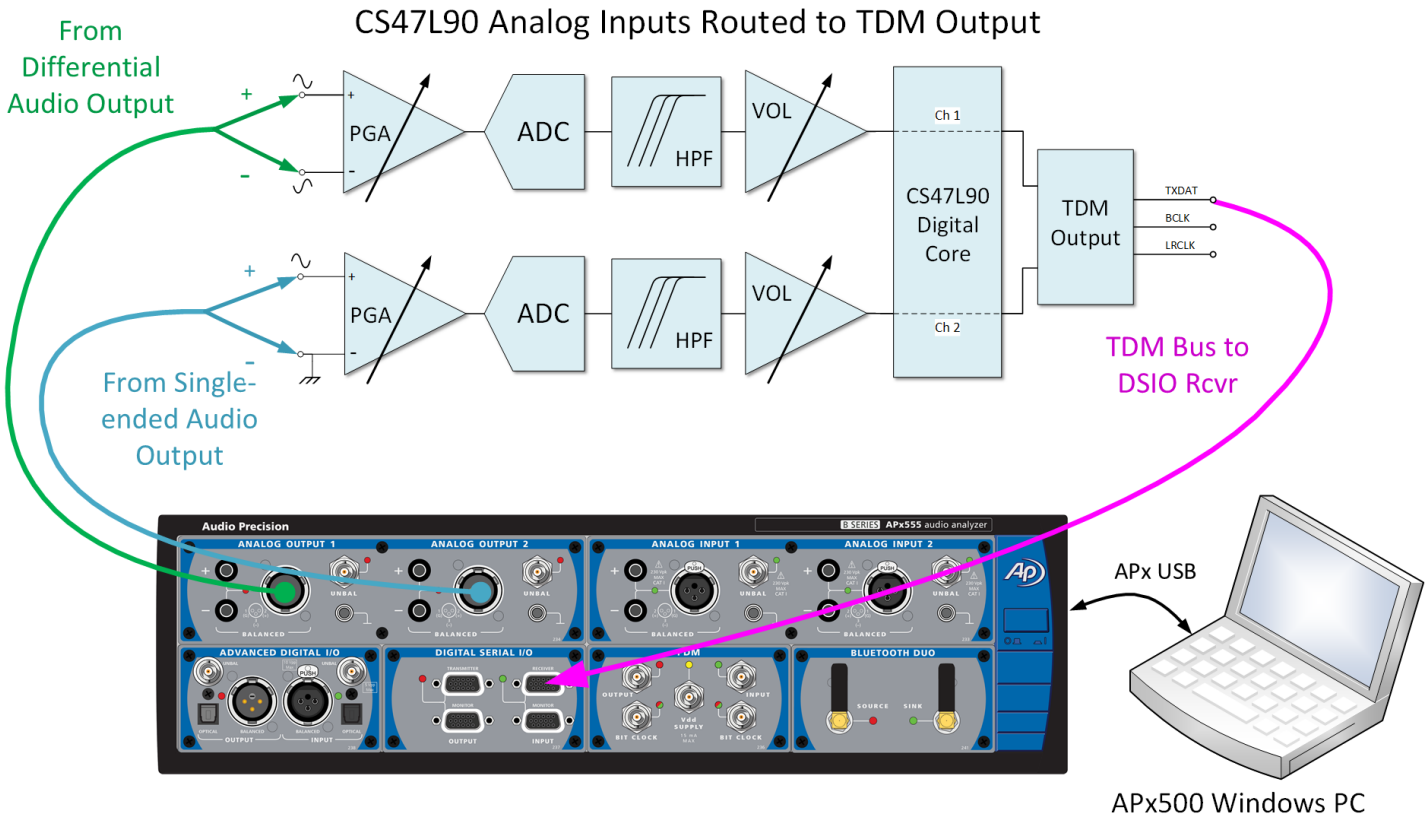

Figure 4. B Series APx555 audio analyzer system signal connections to test the CS47L90 analog inputs and receive digital outputs. The converter's digital outputs are internally routed to one of its TDM outputs.

Figure 5 shows the benchtop setup with the evaluation board and the APx555 audio analyzer connections.

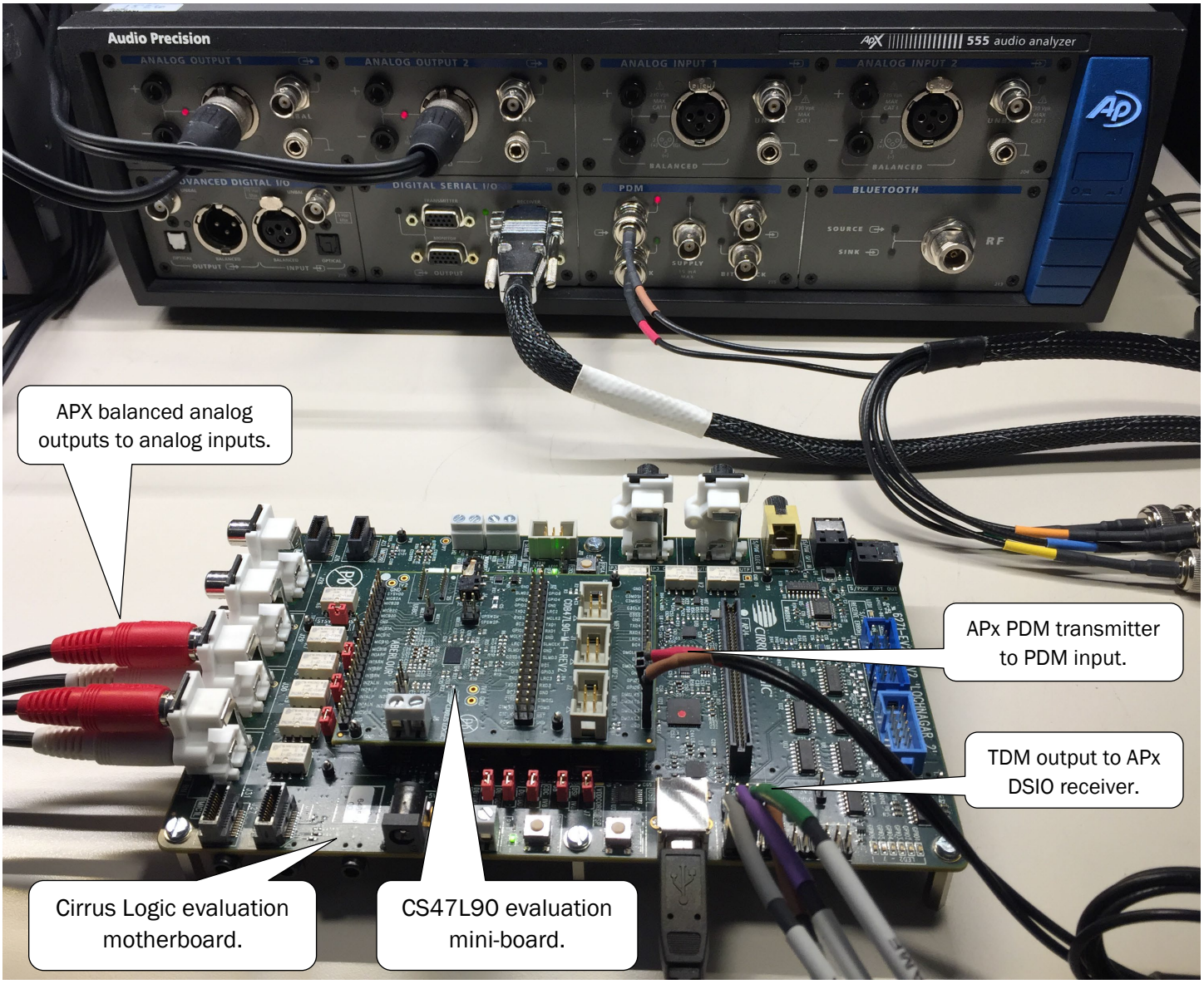

Figure 5. Physical setup for testing a Cirrus Logic CS47L90 evaluation mini-board. The mini-board plugs into the motherboard. The APx555 is connected to the motherboard analog inputs at the left, to the motherboard TDM output at the right, and to the mini-board PDM input in the center. The analog inputs have been modified for DC coupling. The motherboard supplies power and control logic via the USB ports and Cirrus Logic WISCE software running on a PC.

The APx555 can test the device's analog inputs simultaneously by configuring balanced analog outputs to correspond:

• Input/Output
  ○ Analog Balanced (ADC Test)
  ○ VBias: 0.900 V
  ▪ Pin Voltage Protection: ON
  ▪ Pin Voltage Max: 1.800 V
  ▪ Pin Voltage Min: 0.000 V
  ▪ VBias enable: ON
	• Output Settings
	  ○ Config Track Ch 1: Off
	  ○ Ch 1 Configuration: Normal (Differential)
	  ○ Ch 2 Configuration: Single-Ended
	• Generator
	  ○ Waveform: High Performance Sine Generator
	  ○ Precision Tune: ON
	  ○ Levels Track Ch 1: OFF
	  ○ Ch 1 Level: 50 mVrms
	  ○ Ch 2 Level: 500 mVrms
	  ○ Frequency: 1.0000 kHz

Figure 6 shows the corresponding APx500 software settings for the APx555.

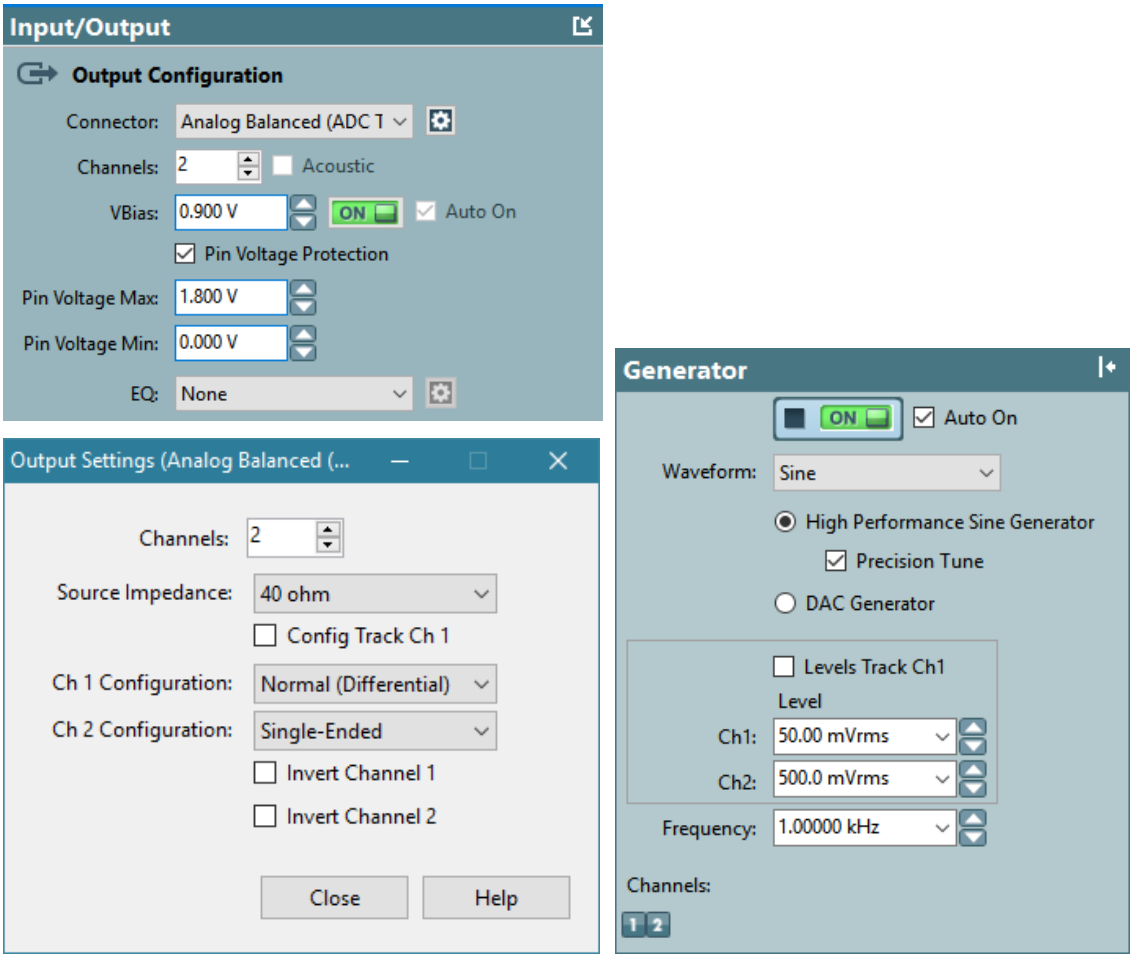

Figure 6. The APx555 analog generator balanced outputs may be configured individually: Channel 1 is configured for differential operation with 50 mVrms (–26.021 dBV) output level (right) and Channel 2 is configured for single-ended operation with 500 mVrms (–6.021 dBV) output level.

DC Coupled ADC Measurements

DC coupled measurements permit characterization of the full operating range of the device's analog inputs including low frequency behavior that would be impossible to measure with an input AC coupling capacitor. DC coupled measurements require an input bias voltage set to ½ V_{DD}. APx555 provides this with the VBias set to +0.9 V.

Gain, Level, and THD+N Distortion Measurements

The APx500 gain and level measurement meters in Figure 7 show that the 50 mV and 500 mV sine wave signals applied to the differential and single-ended inputs results in full scale digital outputs near 0 dBFS, gain of 26 dBFS/Vrms (x20) for channel 1 and 0 dBFS/Vrms (x1) for channel 2, DC Levels very close to 0, and THD+N distortion below −80 dB (observed in the FFT as principally 2nd and 3rd harmonic distortion and noise). In this example, VBias was adjusted to +0.918 volts to achieve the lowest output DC offset in the single-ended channel 2 measurement.

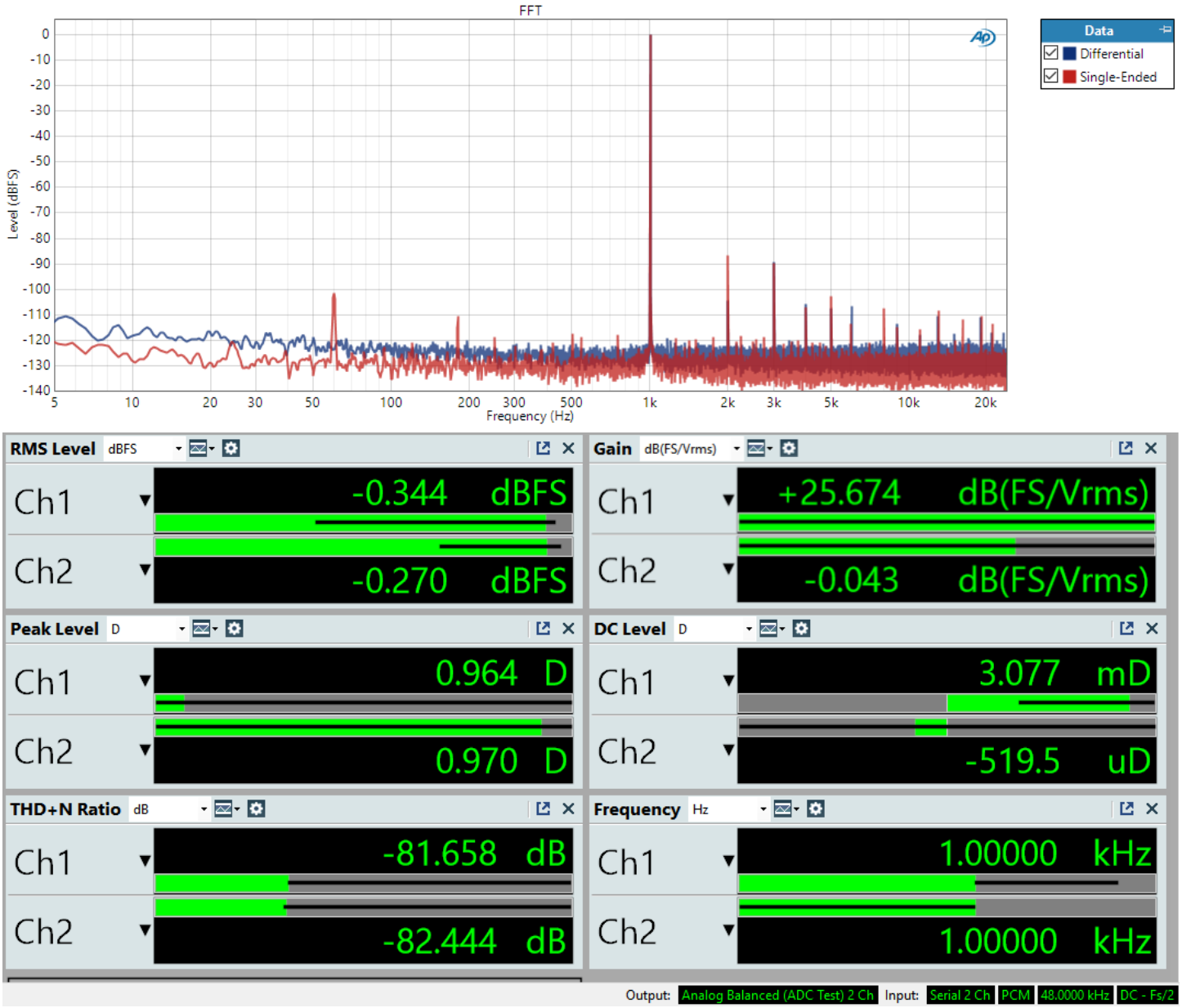

Figure 7. Meter measurements of the digital output from the CS47L90 with 50 mV and 500 mV sine waves applied to the converter inputs.

High Pass Filter Cutoff

The DC connection to the analog inputs simplifies testing high pass filter low frequency roll-off characteristics shown in the Figure 3 block diagram. These filters should not be measured with the usual in-circuit AC coupling capacitors (on the evaluation motherboard) because the 1 µF capacitor time constant will affect the measurement result. A VBias voltage is required if the coupling capacitor is removed.

Figure 8 shows the results from a DC-coupled continuous sweep frequency response measurement. The CS47L90 high pass filter was set to each of the HPF filter settings for these frequency sweep measurement traces. Sweeps were appended to the graph for each filter setting.

All filter settings resulted in < −3 dB attenuation at each filter frequency setting. The ½ V_{DD} VBias voltage makes it possible to DC-couple these inputs to make accurate measurements without a DC blocking capacitor.

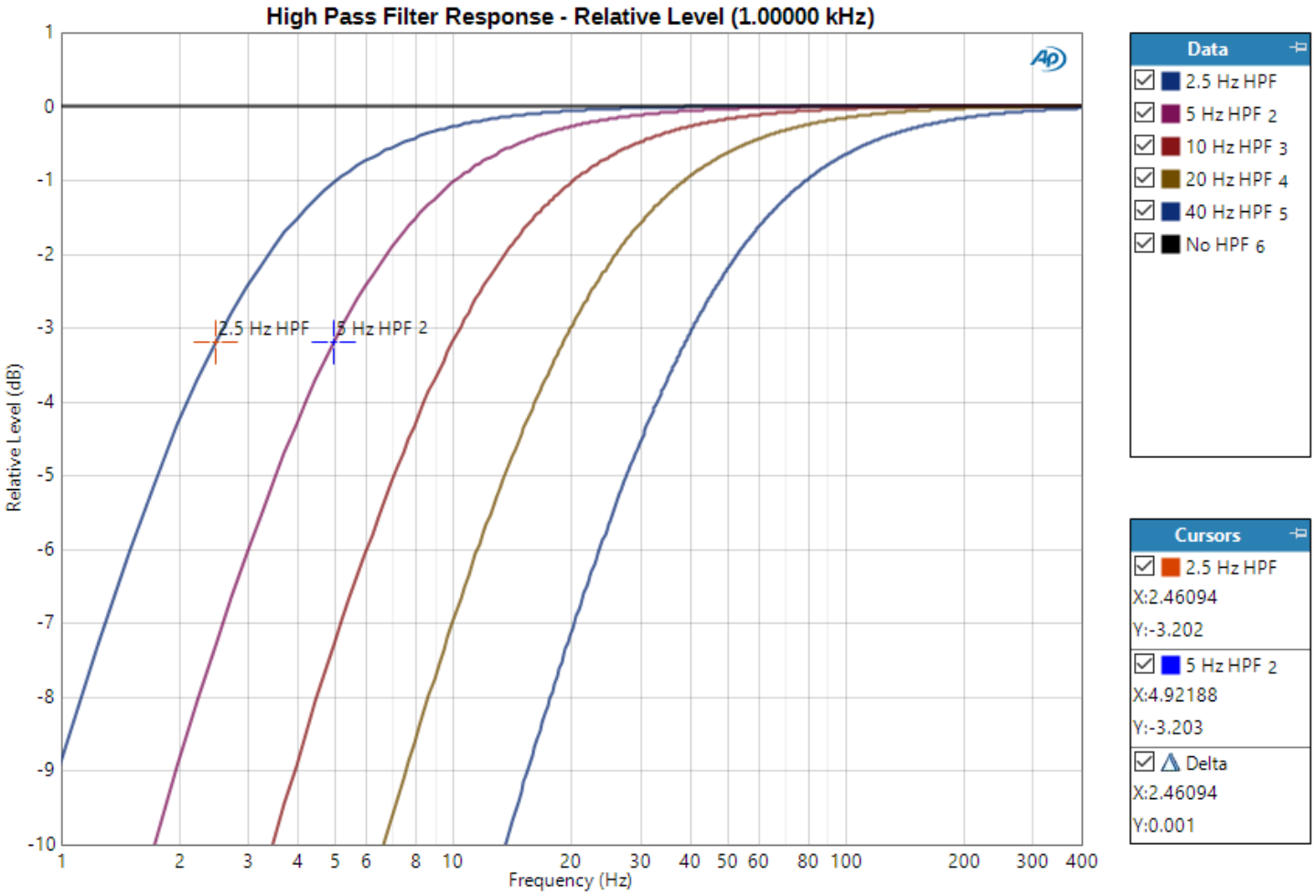

Figure 8. Analog input High Pass Filter response measurement curves from a DC-coupled Continuous Sweep measurement, swept from 1 Hz to 1.0 kHz for each setting of the CS47L90 high pass filters at 44.1 kHz sample rate. All filter frequency settings resulted in < −3 dB at the cutoff frequency.

Single-Ended DC Coupled Dynamic Range Measurements with VBias Sweep

Dynamic Range (DNR) can be measured as a function of DC offset in a single-ended analog input by applying a low distortion −60 dBFS sinewave (500 µVrms), performing a Bench Mode stepped level sweep of VBias, and measuring THD+N Level with appropriate measurement filters (CCIR-2K filter, 20 Hz High Pass, and 20 kHz Low Pass). Make the measurement for each value of VBias voltage from 0 VDC to V_{DD} in 5.0 mV steps. The APx500 software Bench mode can sweep the VBias voltage value to accomplish this.

The APx500 Bench Mode settings are shown in Figure 9.

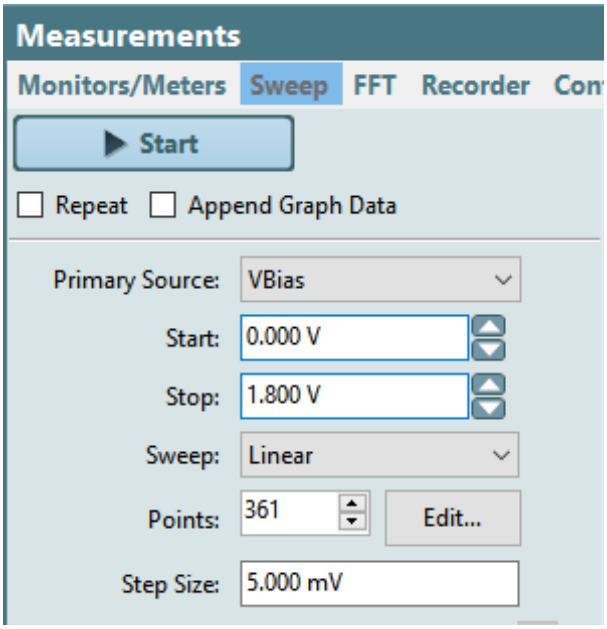

Figure 9. Bench mode settings for a sweep of VBias from 0.0 V to 1.8 V in 5 mV steps.

The result graphs DNR versus VBias (Figure 10). The graph shows optimal dynamic range performance with VBias set near 0.9 V (½ V_{DD}) and non-linear behavior for values below 0.2 V and above 1.645 V.

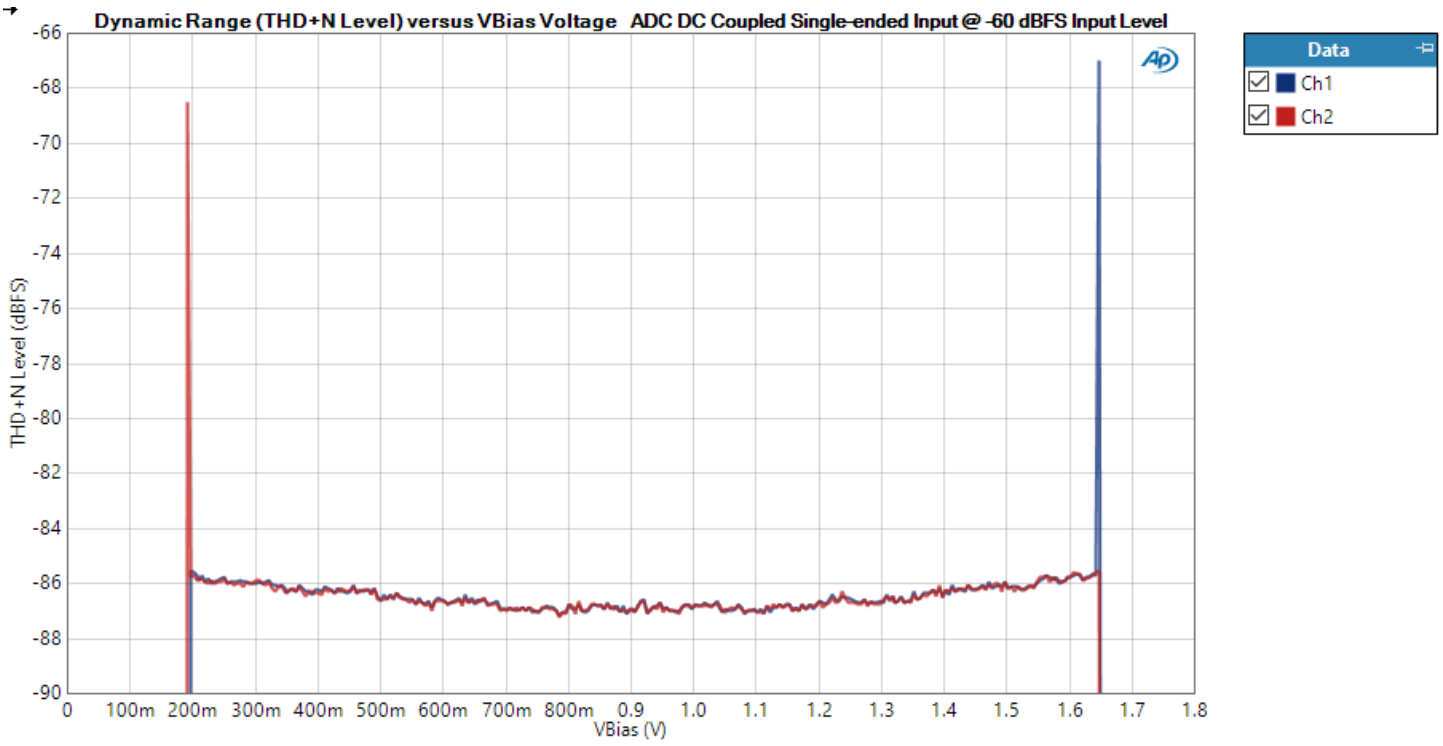

Figure 10. Measurements of CS47L90 single-ended analog input DNR as a function of VBias DC offset with −60 dBFS (1 mV) 1 kHz sine wave input. VBias swept from 0.0 V to +1.8 V (V_{DD}). Measurement bandwidth: 20 Hz to 20 kHz, CCIR-2K weighting filter.

Differential DC Coupled Dynamic Range Measurements with VBias Sweep

Dynamic Range as a function of DC offset for a differential analog input can also be performed with the same technique. Drive the differential input with a low distortion −60 dBFS sinewave (1.0 mVrms) from the APx555 analog output configured for differential and measure THD+N Level with CCIR-2K filter, 20 Hz High Pass and 20 kHz Low Pass measurement filters.

Make the measurement for each value of VBias voltage from −0.4 VDC to V_{DD} in 5.0 mV steps. The result is a graph of DNR versus VBias (Figure 11). The graph shows best performance with VBias as low as −0.4 V and up to 1.6 V before distortion begins to increase as VBias approaches V_{DD} at the right.

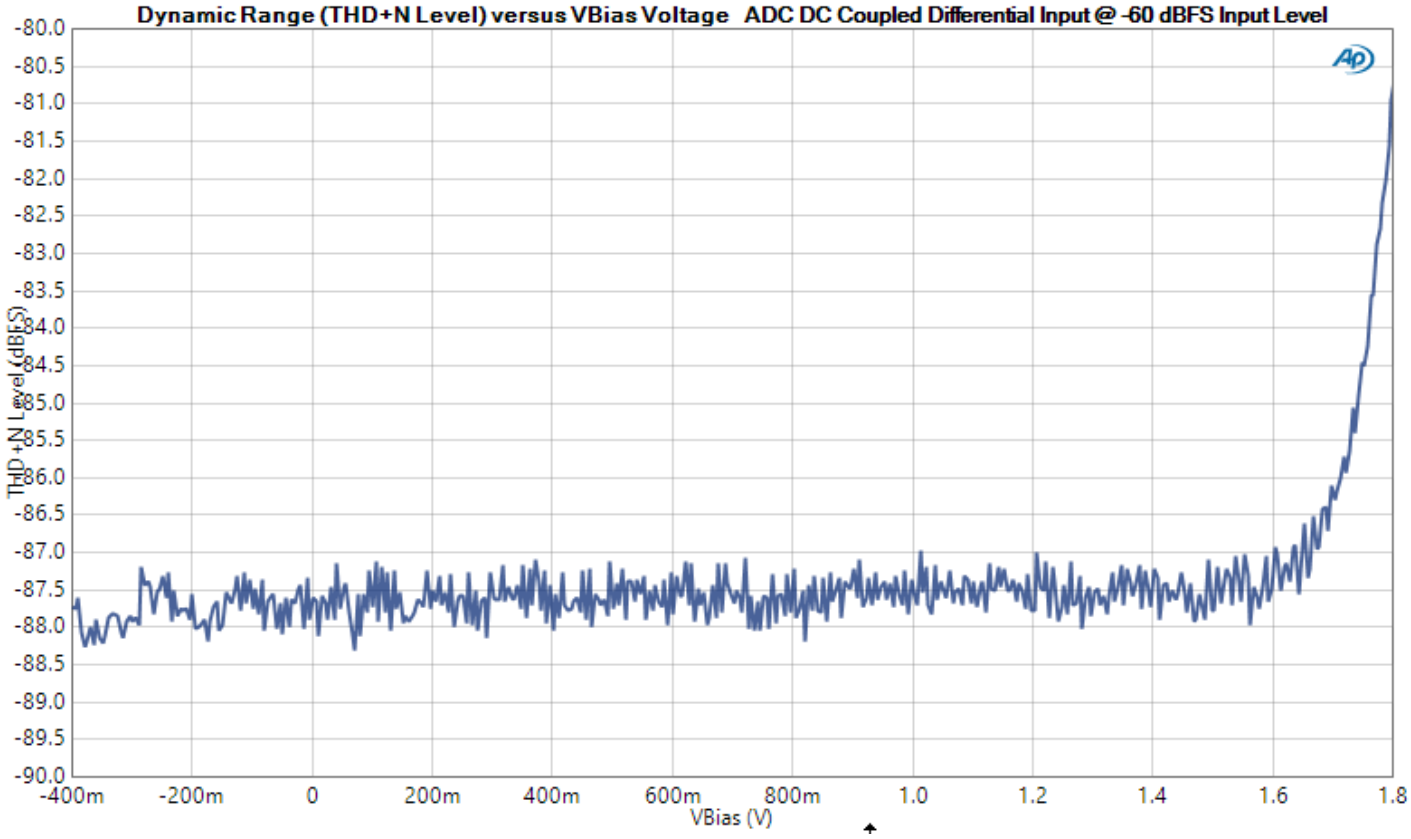

Figure 11. Measurements of CS47L90 differential analog input DNR as a function of VBias DC offset with −60 dBFS (1 mV) 1 kHz sinewave input. VBias swept from −0.40 V to +1.8 V (V_{DD}). Measurement bandwidth: 20 Hz to 20 kHz, CCIR-2K weighting filter.

Simultaneous Analog and Digital Output

The APx555 analog high-performance sine wave generator hardware can be used simultaneously with any digital audio output interface, such as the PDM or TDM outputs. The high-performance sine wave generator is an analog oscillator that can operate independently of the digital generator. The Analog Sine Generator can be operated while the PDM output is active.

This is very useful for testing analog inputs while applying high frequency PDM signals to nearby pins in the analog subsystem of the chip. Interference or noise from the PDM inputs will be easily measured in the converter outputs routed through the chip to the TDM inputs of the APx555B.

Figure 12 illustrates this configuration of the IC. The input signals are routed through the digital core for output through a TDM port. In this example, the TDM stream carries four audio channels: Ch 1 from the ADC with the differential audio input, Ch 2 from the ADC with the single-ended audio input, and channels 3 and 4 from a stereo digital microphone input.

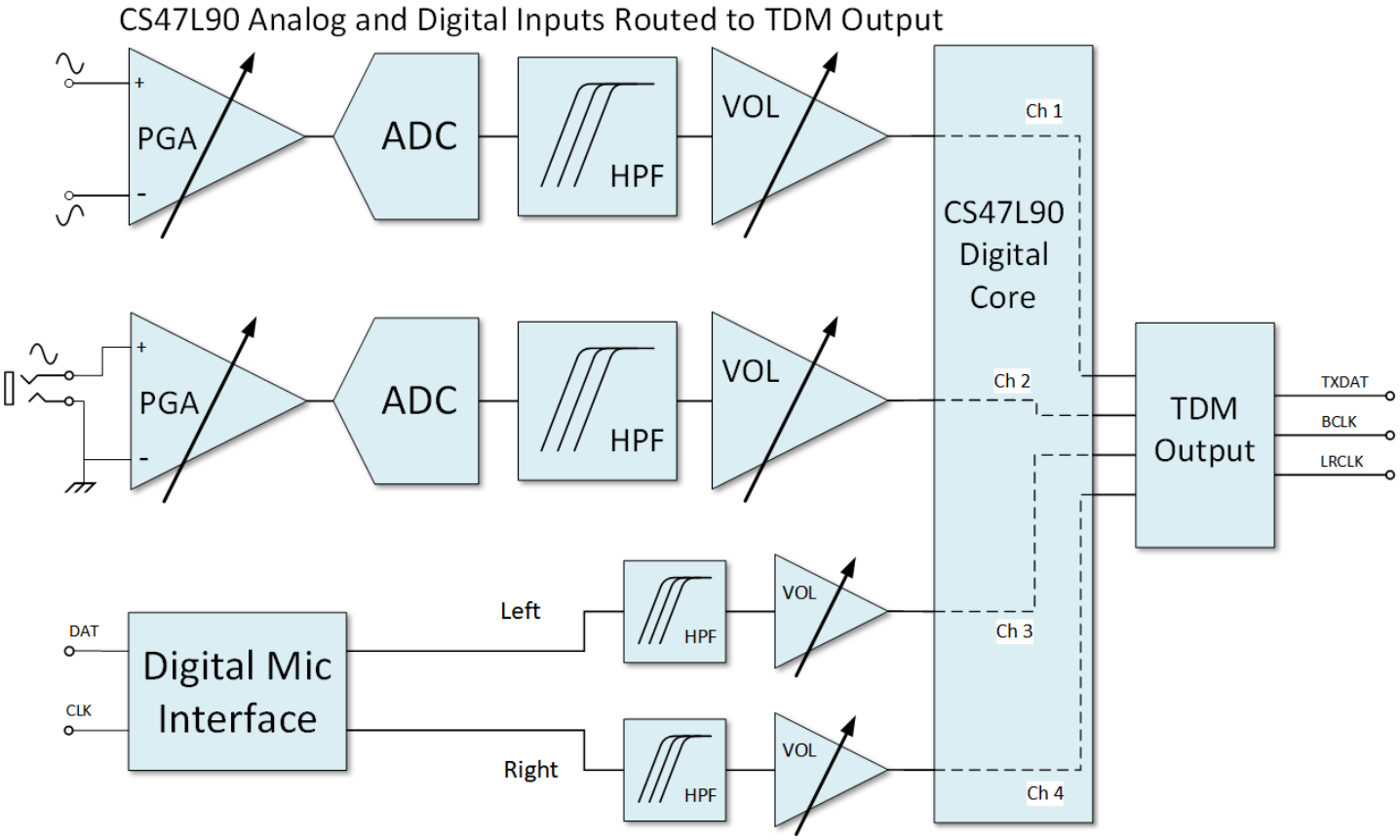

Figure 12. CS47L90 block diagram of analog and PDM digital inputs routed to a TDM output.

Figure 13 illustrates the signal connections between the APx555 and the CS47L90 analog inputs, PDM input, and TDM output.

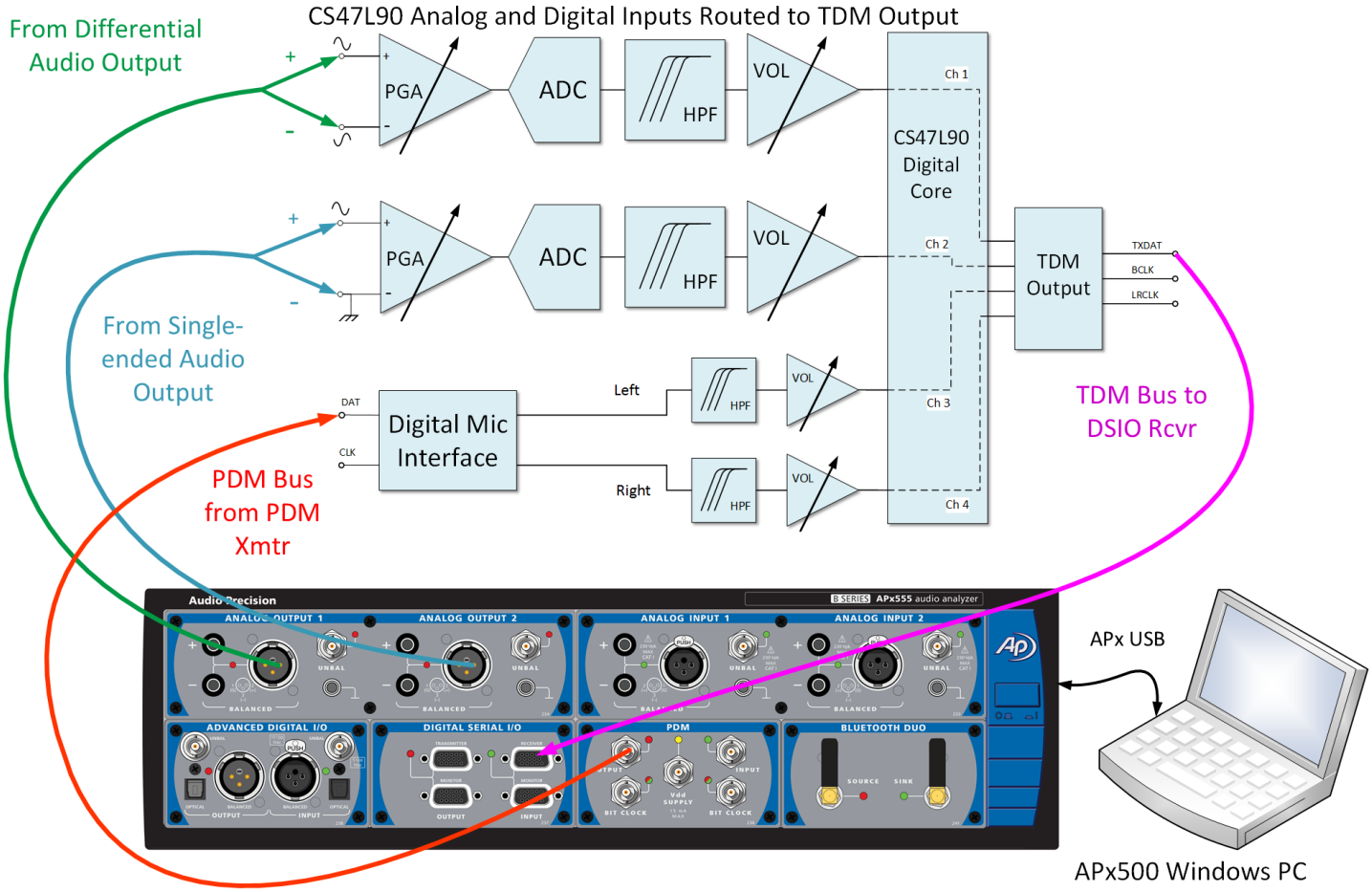

Figure 13. Block diagram of the APx555 audio analyzer test system for the CS47L90 evaluation board.

The basic setup is shown in the APx500 software Bench mode screen capture in Figure 14.

To set this up:

1. Set the Output Configuration to PDM to enable PDM output from the APx555 to the IC's digital mic input. Then complete the PDM transmitter setup.
2. Select the toolbar button to display the Analog Sine Generator control panel to configure and enable analog output from the APx555 to the IC's analog inputs. The Analog Sine Generator control panel can be closed or moved on the screen after setup is complete.
3. Set the Input configuration to Digital Serial to enable the APx555 DSIO receiver connected to the TDM digital output of the IC. Then complete the DSIO receiver setup.

The CS47L90 evaluation board connections to the APX555 are shown in Figure 5.

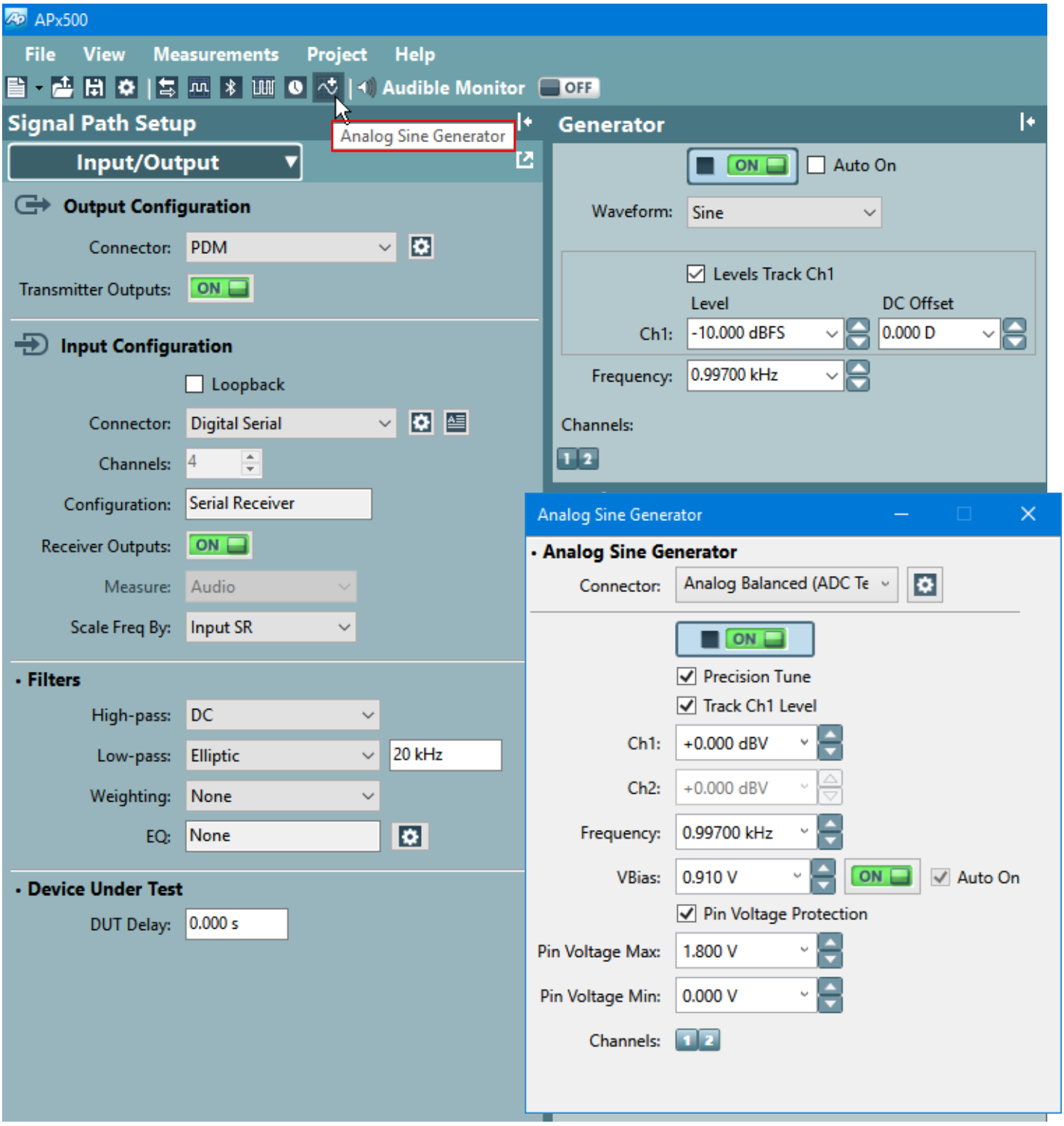

Figure 14. APx500 Bench mode controls for simultaneous analog and digital output.

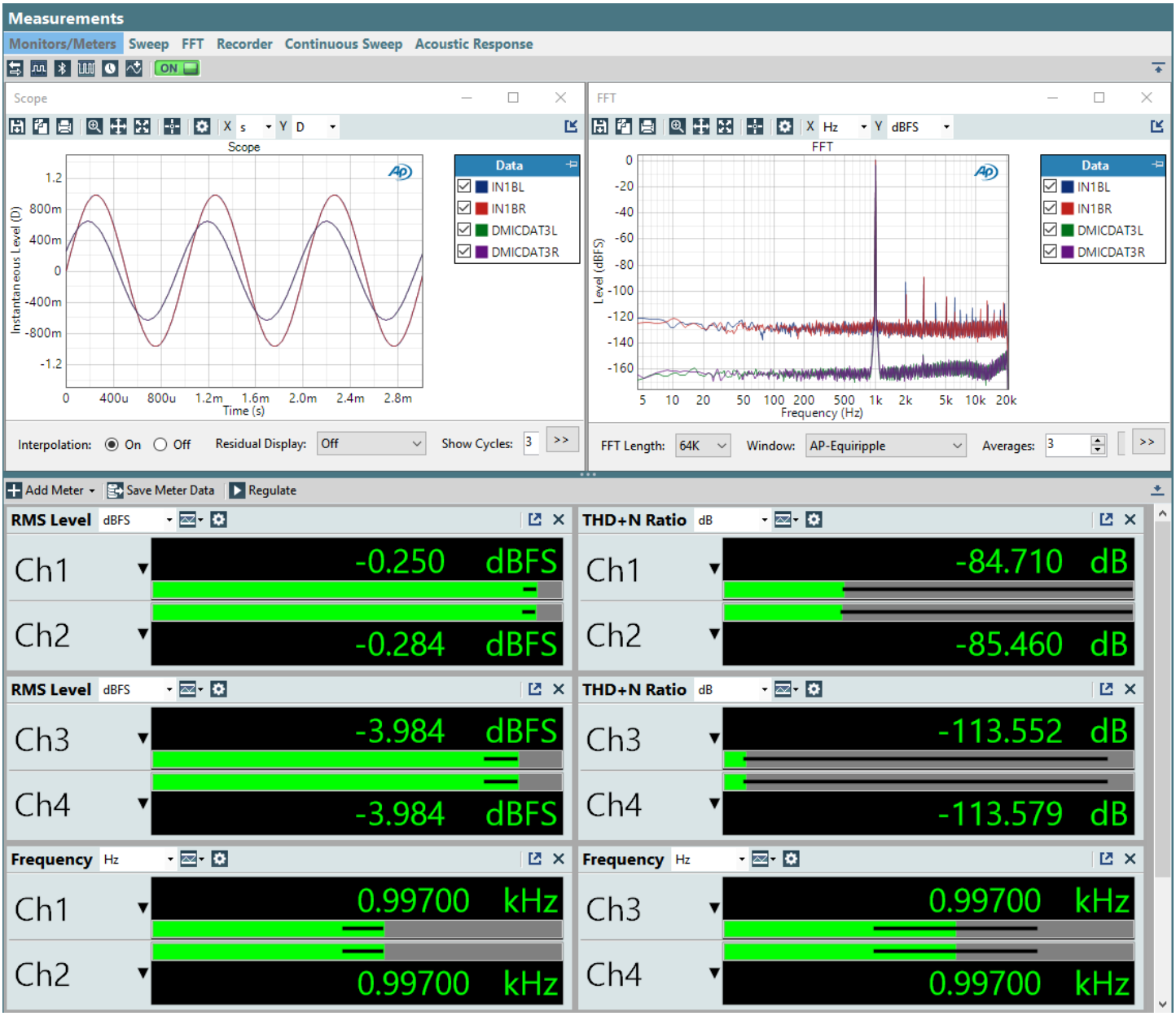

Figure 15. Measurements of the CS47L90 four-channel TDM output with simultaneous analog and PDM inputs. CH1=IN1BL, CH2=IN1BR, CH3=DMICDAT3L, CH4=DMICDAT3R. The upper FFT traces are the analog inputs.

APx500 Project Files

These APx500 project files are provided in the zip file for Technote 136. They are compatible with APx500 software version 5.0 and later and require either a B Series APx555 or a Legacy APx555 with the EAG upgrade. Additionally, the APx555 must be equipped with the ADC Test option and DSIO module.

Filename	Title	Description
TN136-1.approjx	ADC Simultaneous Differential & Single-ended Input Measurements in Sequence Mode	Performs sequence mode measurements and generates a report file. **APx500 settings:** Balanced analog output and DSIO I2S input @ 48 kHz sample rate (master bit and frame clock outputs). Ch1 differential output @ 50 mVrms with 0.9 V VBias. Ch2 single-ended output @ 500 mVrms with 0.9 V VBias.
TN136-2.approjx	ADC Low Frequency High Pass Filter Response Measurements	Sequence Mode measurements of DC-coupled differential input ADC. Measures frequency response from 1 Hz to 1.25 kHz. **APx500 settings:** Balanced analog output and DSIO I2S input @ 48 kHz sample rate (master bit and frame clock outputs). Ch1 & Ch2 analog differential output @ 1.0 Vrms with 0.9 V VBias.
TN136-3.approjx	ADC Differential Input Distortion Measurements versus VBias Voltage	Bench mode measurements of DC-coupled differential input ADC. Measures channels 1 & 2 THD+N Level distortion as a function of VBias voltage from −0.4 V to 1.8 V. **APx500 settings:** Balanced analog output differential configuration and DSIO I2S input @ 48 kHz sample rate (master bit and frame clock outputs). Ch1 & Ch2 analog differential output @ 1.0 mVrms (−60 dBFS) with swept VBias.
TN136-4.approjx	ADC Single-ended Input Distortion Measurements versus VBias Voltage	Bench mode measurements of DC-coupled single-ended input ADC. Measures Distortion as a function of VBias voltage from −0.0 V to 1.8 V. **APx500 settings:** Balanced analog output single-ended configuration and DSIO I2S input @ 48 kHz sample rate (master bit and frame clock outputs). Ch1 & Ch2 analog single-ended output @ 1.0 mVrms (−60 dBFS) with swept VBias.
TN136-5.approjx	Measurements of ADC 2-channel Differential Analog Inputs Simultaneous with PDM 2-channel Input via 4-channel TDM serial output.	Bench Mode measurements shown in Figure 15. Sequence Mode measurements of Level and Gain, THD+N, Frequency, Continuous Sweep, Stepped Frequency Sweep, Noise (RMS), Dynamic Range – AES17, Signal Analyzer (FFT), DC Level, Crosstalk. **APx500 settings:** Balanced analog output differential configuration with 1 Vrms 2-channel output with 0.9 VBias. 2-channel 48 kHz PDM Output to DUT Digital Microphone input. DSIO receives 4-channel TDM input from DUT @ 48 kHz sample rate and provides master bit and frame clock outputs.

5750 SW Arctic Drive, Beaverton, Oregon 97005 | 503-627-0832

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